THYCON

Est.1968

Solid State Breaker

SSB 600 – 4000A

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Solid State Breakers

SSB | 0.6 - 3.0MVA

History

Solid-state switches have been in use for many years in both AC and DC circuits, and take many forms; they offer the following benefits:

- IGCTs interrupt current in about 1 microsecond (10 – 20us including fault information acquisition and control response)
- no arcing, no moving parts, no gasses or oils (no maintenance)
- silent interruption
- multiple fast re-closure for line-fault presence-verification (in kHz range)
- prospective fault current can be limited to <10% of that of mechanical breakers
- limited fault current reduces mechanical cable stress (reduced maintenance)
- new technology with development and cost-reduction potential.

Principal of Operation

The simplest systems use back-to-back thyristors which, when the gate signals are suppressed, simply block the current when it commutates naturally to zero in an AC circuit, as shown in Fig.1. Such systems can take up to one half cycle to block a fault current (i.e. up to 10ms in a 50Hz network). Because of zero-current interruption (the thyristors turn off like diodes, there is little stress on the switch and little energy to be absorbed. A snubber protects the thyristors from the overvoltage which is caused by the reverse-recovery current flowing backwards during the thyristor's reverse recovery time but this represents only a small amount of energy due to the small reverse recovery current of the thyristor (Fig. 2).

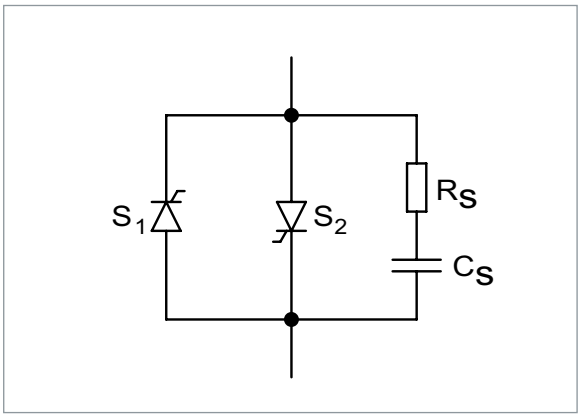

Fig. 1 Solid-state AC interrupter composed of two thyristors

In Fig. 2, the forward current (not fully shown) is the fault current. The recovery time tRR of one or two microseconds is a characteristic of all bipolar semiconductors and causes the reverse current IRR to reach a few tens of amps. The snubber circuit (RS/CS) absorbs the energy resulting from 0.5 x IRR2 x L where L is the circuit inductance. With this kind of breaker, there are no arcs and very little energy is dissipated on interruption. The life expectance of the breaker itself is virtually unlimited and maintenance involves no more than periodic cleaning.

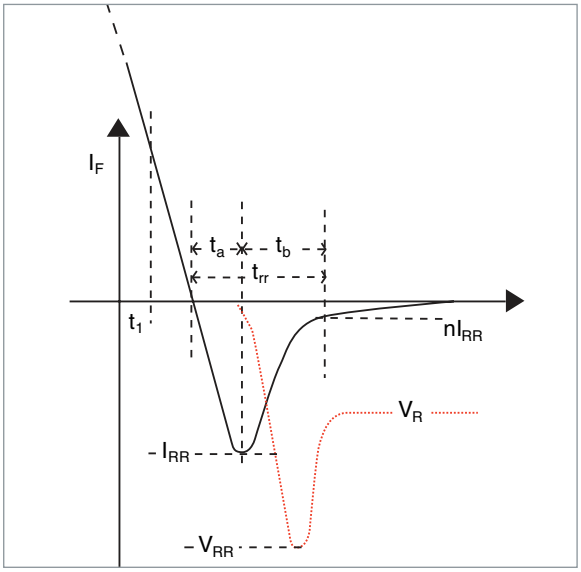

Fig. 2 Reverse recovery of a line-commutated thyristor

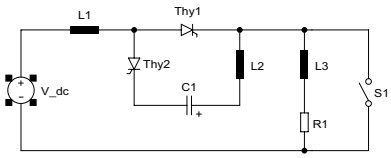

Fig. 3 – DC breaker using a force-commutated thyristor

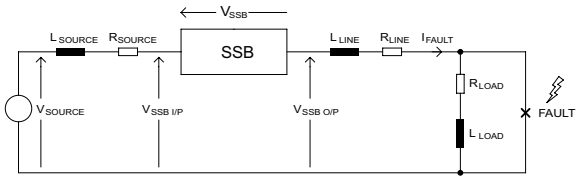

Fig. 4 – AC SSB in its environment

Forced turn-off static breakers

Although the maintenance on the semiconductors is negligible, this kind of fault, if repeated too frequently, will put mechanical stress on the cable and connections which may require regular inspection.

Clearly, an ideal breaker would intelligently assess when a current is unacceptably high and interrupt the current long before it attains such mechanically stressful levels.

Forced (as opposed to naturally) commutated breakers achieve sub-cycle switching. These can be realised using forced-commutated thyristors or self commutated or Turn-off Devices (ToDs) such as GTOs, IGBTs, IGCTs, ETOs, etc. An example of this is shown in Fig. 3 for a DC breaker using force-commutated thyristors.

In this figure, the supply voltage is V_dc, L1 represents the source and line inductance, L3/R1 represent the normal load which is shorted by the fault at switch S1. The thyristor Thy1 carries the normal load current. When a fault current is detected, Thy2 is fired which applies the voltage on C1 to the cathode of Thy1 forcing the current to zero through inductance L2. Current is thus diverted from Thy1 to Thy2 and C1 gets charged in the opposite direction, subsequently turning off Thy2 and thus interrupting the current. The energy stored in L1 is transferred to C1.

C1 must always be charged to the polarity shown when Thy1 is conducting (SSB ON) and thus requires a small isolated power supply to keep it charged; this same power supply can be used to discharge the capacitor from its negative charge state after a current interruption. The size of C1 is determined by the value of L1, the programmed current interruption level and the characteristics of the thyristor Thy1 and L2 is determined principally by C1.

Breakers with self-commutated devices

A conceptually simpler approach uses ToDs devices, such as the afore-mentioned GTOs, IGBTs etc. A typical application is shown in Fig. 4.

Fig. 4 is more detailed than the previous example as it shows both the source impedance and the line impedance up to the point of failure which could be anywhere along the distribution line.

Static interrupter

SSB performance in a typical AC power network

The assumed single phase configuration for this simulation is shown in Fig. 4 where a typical generator represents Vsource. “Fault”, represents the fault on the utility bus. The purpose of the SSB is to isolate the generator from the fault.

The source inductance of Fig. 4 is that of a single machine rated 620kVA/415V where INOM = 863ARMS. Assuming 10% continuous overload capability, this corresponds to a continuous current of 950ARMS. The real power of the generator is 496kW so it operates at a PF of 496/620 = 0.8.

Assuming a 0.1 p.u. reactance, the symmetric fault current for this machine would be 9500ARMS which corresponds to an asymmetric peak of 27kA

Set the circuit elements to the following arbitrary values:

LLINE = 100uH, RLINE = 0.1mOhm
LSOURCE = 140uH RSOURCE = 1mOhm
LLOAD = 834uH, RLOAD = 0.35Ohm

These are used in the simulation circuit of Fig 4 with the additional assumptions:

1. the fault occurs at voltage zero during steady-state FL operation
2. the line voltage is set to 415V + 12.5%, 50Hz
3. the current sensor has a 2us delay, the control circuit has a 6us delay and the ToD an 8us delay = 16us total delay
4. the trip level is set at:
   FLC + 50% overload + 20% margin = √2 x 950 x 1.5 x 1.2 = 2400A.
   The simulation results are shown in Figs 5 and 6.

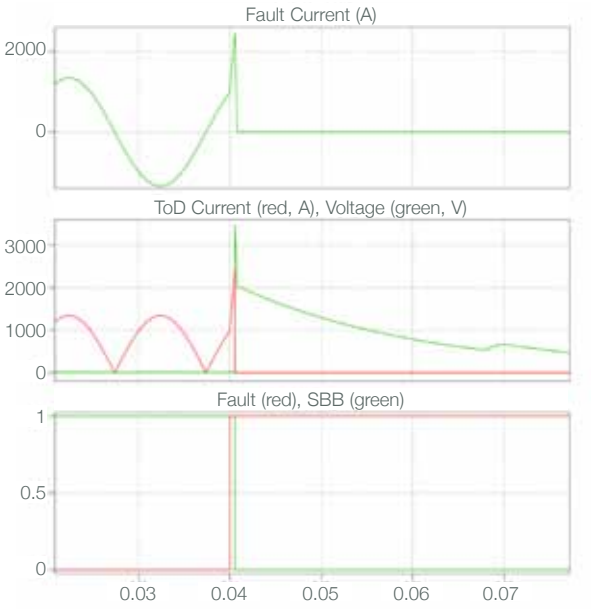

Fig. 5 – Fault current (top trace), ToD current and voltage (centre traces) and fault and turn-off signals (lower traces). Circuit has prospective symmetric fault current of 9.5kARMS

Fig. 5 shows that the steady-state peak load current through the SSB prior to the fault is 1343A (=√2 x 950A) and that the period between the fault occurrence and the SBB turn-off signal (lower traces) is 0.54ms.

Expanding the waveform of Fig. 5 around the current interruption point, we obtain the oscillogram of Fig. 6 from which we see that the fault current barely reaches 2442A (for a trip setting of 2400A) and that the time between tripping and falling to zero of the current is 0.29ms during which time the decaying fault current commutates from the ToD, to the snubber and then to the varistor. The peak voltage across the SSB is 3462V and for this reason, a 4.5kV ToD is chosen. The current in the ToD itself falls extremely quickly (in about 6.5us) but the total current in the SSB takes the aforementioned 0.29ms to decay to zero of which the bulk is taken up by varistor conduction.

The energy absorbed (not shown) by the snubber resistance is found to be 4.5J, that by the varistor is 900J (and that by the IGCT is about 19J – from data-sheet, not shown), i.e. a total energy of 924J. The initially stored energy was 0.5 x 0.24mH x 24422 = 715J so an additional 208J were drawn from the supply during the time that the breaker voltage (not shown) remained below the line voltage.

The voltages to, from and across the SSB are shown in Fig. 7 from which it can be seen that the peak VSSB I/P voltage reaches 2925V, that across the SSB reaches 2290V (VSSB) and VSSB O/P only attains 1172V (= 3515 – 2925). This situation is unchanged when the fault occurs in the opposite direction (not shown). Thus, the supply voltage must be capable of withstanding transient voltages of about 3kV for about 0.26ms but the output voltage to the distribution network sees no more than 1200V, in compliance with AS 4777.2—2005.

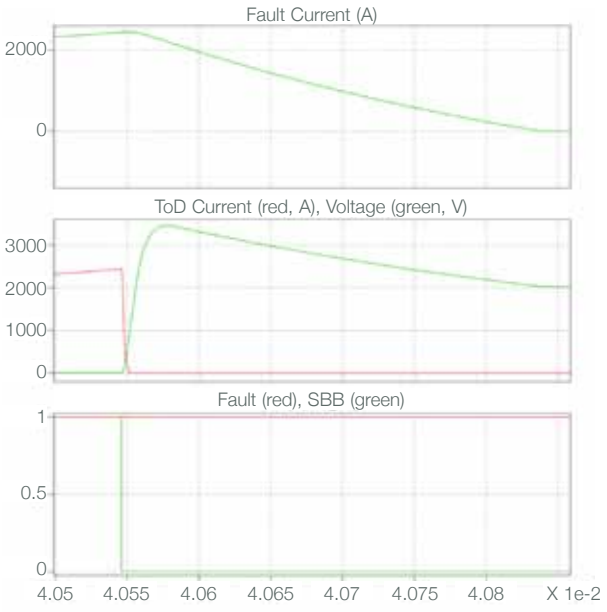

Fig. 6 – Expansion of Fig. 5

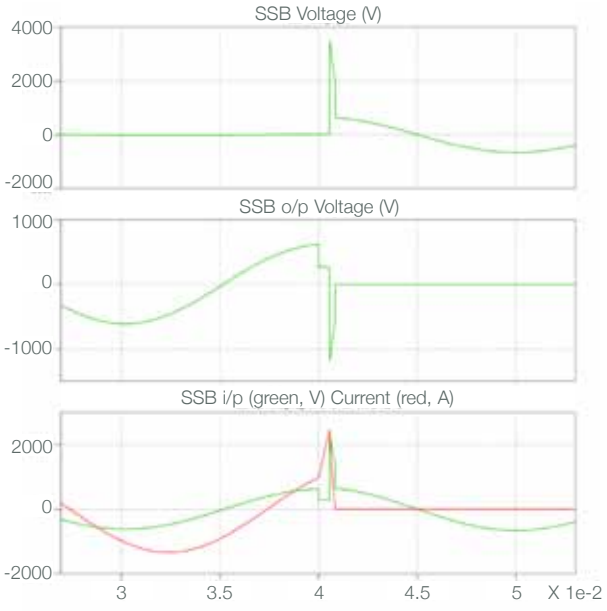

Fig. 7 – Voltage across SSB (top trace), line o/p voltage from SSB (centre trace) and line i/p voltage to SSB and fault current (lower traces)

It can be seen from the foregoing that:

1. an SSB can limit the fault amplitude to practically the set trip-level even when the fault occurs at zero voltage (worst case) and where the prospective fault current is high
2. the SSB imposes no over-voltages on the o/p line
3. the fault has a very short duration of about 0.3ms
4. there are no arcs nor mechanical stresses
5. the fault amplitude is virtually unrelated to the circuit prospective fault current.

Reliability and protection

SSBs use semiconductor devices as switches. These are the same devices as are currently used in many high-power high reliability applications such as Uninterruptible Power Supplies (UPS), Wind Power converters and Traction drives. In such applications, semiconductors are used in switching mode i.e. they switch current on and then switch off to block voltage and do so hundreds of times per second. Under such conditions they are subject to turn-on, turn-off and leakage current losses and undergo stresses from the simultaneous transient presence of current and voltage. Nevertheless, these devices are used in very high power high reliability applications with life expectancies of 20 to 40 years.

In the SSB application, the same devices are used to conduct current only during most of their lifetimes and switch only once a day to once a year (depending on fault occurrences). This application is thus one of the most reliable that can be found for power semiconductors since they are subject to so little stress.

Nevertheless, for reasons of isolation and contingency, an SSB may be fitted with an additional fuse in an isolating fuse holder. The fuse characteristics would be co-ordinated with the worst-case protection function in the event of an SSB failure. For this (as for the overall design) the protection philosophy of the system needs to be defined and the characteristics of the circuit (impedances) as well as the characteristics of other protection devices need to be known.

Conclusion

In short, in can be said that, SSBs:

- are fast, silent and arc-free
- interrupt current close to the fault detection (trip) level
- have a let-through current which is extremely small (trip level x 0.3ms) and is independent of prospective fault level
- can be modular and series-connected for higher voltage or parallel-connected for higher current
- can be made for AC and DC operation with identical performance
- are quasi maintenance-free
- can be programmed for automatic verification
- have unlimited lifetime (≈ 30 years)

Thycon has 30 years of experience in high power electronics for the Australian environment and the Thycon SSB applies little overvoltage to the network and complies with AS 4777.2—2005.

Technical specification

SSB (three phase)				
Single unit rating	600kVA	1000kVA	1500kVA	3000kVA
Efficiency (%)	99	99	99	99
Interruption time	Circuit dependant. Typically 10-300uS			
Fault capability (kA)	<50	<50	<50	<50
Foot print (wxdxh)	1200x1000 x2000	1200x1000 x2000	1600x1000 x2000	2000x1000 x2000

Specification is subject to change without prior notice

THYCON

THYCON INDUSTRIAL PTY LTD
20 Audrey Ave Coburg
3058 VIC Australia
PH 61 3 9319 9000
FAX 61 3 9319 9001
ABN 17 068 011 049
www.thycon.com.au
info@thycon.com.au

24 HR Service Australia
1800 670 700